JSS MAHAVIDYAPEETHA

JSS ACADEMY OF TECHNICAL EDUCATION

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1. **NAME** : Mrs. Saroja S Bhusrae
2. **Designation** : **Assistant Professor**
3. **Name of the Dept.** :**Electronics and Communication Engineering**
4. **Date of joining the Institution: 28-01-1999**
5. **Date of Birth** : 03-03-1974
6. **Father's Name** Siddaramappa Bhusare
7. **Sex** : Female
8. **Nationality** : INDIAN
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Bangalore-98

11. **Employment Type** : Permanent
12. **Educational Qualifications** : **B.E., M.Tech., (Ph.D).,**
(In reverse Chronological Order)

Sl.	Degree	Branch	Specialization	Year of passing	University

No.					
1	Ph.D.	Electronics & Communication Engineering	VLSI Design and Embedded Systems	Persuing	VIT, Chennai
2	M.Tech	Electronics & Communication Engineering	VLSI Design and Embedded Systems	2005	VTU, Belagavi
3	B.E.	Electronics & Communication Engineering	Electronics & Communication Engineering	1997	Karnatak University, Dharwad

13. **Service / Experience Details :17.8 years**
(In reverse Chronological Order)

a. Teaching Experience:

Sl. No.	From (mm/yy)	To (mm/yy)	No. of years	Degree or Diploma Institution	Designation	Name of the Institute
1	**13-11-2006**	**Till date**	**9.10 years**	**Degree**	**Assistant Professor**	**JSS Academy of Technical Education, Bengaluru 560 060**
2	**25-06-2005**	**12-11-2006**	**1.5**	**Degree**	**Senior Leturer**	**JSS Academy of Technical Education, Bengaluru 560 060**
3	**28-01-1998**	**24-06-2005**	**6.5**	**Degree**	**Lecturer**	**JSS Academy of Technical Education, Bengaluru 560 060**
Total Experience			**17.8 Years**			

b. Industrial Experience:

Sl. NO	From	To	No. of years	Designation	Name of the Company

1	**NIL**

14. **Membership in various University Boards / Committees / Other (Specify):**

Sl. No.	**Body**	**From**	**To**	**Name of the University / Institution / Organisation**
1	Board of Examiners			
2	Board of Studies			
3	Academic Senate			
4	Executive Council			
5	LIC MPCC			

15. Awards NIL

16. Details of Books published : NIL

17. Number of Ph.D. Guidance NIL

Field of Expertise / Interest VLSI Design

Low Power Design

Analog VLSI Design

18. Patents : NIL

19. Projects NIL

Sl. No.	**Name of the project**	**Principal Investigator / Co-Investigato**	**Amount sanctioned From**	**Amount**	**Date of start of the project**	**Date of completion of the project**	**Outcome of the project**
1							

2							
3							
4							

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20. Details of Publications:

Google scholar link: https://scholar.google.co.in/citations?view_op=list_works&hl=en&user=7-MyscAAAAAJ

As on 30-08-2016

Citation Indices	**All**	**Since 2011**
Citations		
h-Index		
i10-Index		

Number of papers published in International Journals : 01

Number of papers published in National Journals : NIL

Number of papers published in International Conferences : 02

Number of papers published in National Conferences : NIL

a. Journals: International

Sl. No.	Name of Co-Author	Title of Paper	Name of the Journal	Publisher	Publication citation ISSN, ISBN, Vol. No., Issue, pp
	Dr. V S Kanchana Bhaaskaran	Fixed-Width Multiplier with Simple Compensation Bias	Procedia Materials Science	Science Direct	Volume 10, 2015, Pages 395–402

b. Conferences: International

Sl. No	Name of Co-Author	Title of Paper	Name of the Conference	Publisher	Publication citation ISSN, ISBN, Vol. No., Issue, pp
1	Dr. V S Kanchana Bhaaskaran	Fixed-Width Multiplier with Simple Compensation Bias	2nd International Conference on Nanomaterials and Technologies (CNT 2014)		doi:10.1016/j.mspro.2015.06.071 Volume 10, 2015, Pages 395–402 17th October-2014
2	Dr. V S Kanchana Bhaaskaran	Design of a Low Error Fixed-Width Radix-8 Booth Multiplier	Signal and Image Processing (ICSIP), 2014 Fifth International Conference	IEEE	doi: DOI:10.1109/ICSIP.2014.39 INSPEC Accession Number: 14198996 Month & Year 8-10 Jan.2014 Page Nos. : 206-209

National. Conferences / Symposium / workshops

Sl. No.	Title of the workshop/conference	Duration	Venue	Venue/date
1	Digital Signal Processing and Applications	17 day workshop	UVCE	Bangalore university, UVCE, Dept of Electronics and Communication Engg. Bangalore From 29th July to 14th August 2002
2	A short term course on System C and Applications on VLSI Design	Three day workshop	JSSATE	Dept of Electronics and Communication Engg. JSSATE, Bangalore 6th to 8th April 2005
3	Mixed Signal VLSI	Six day workshop	Bangalore Institute of Technology	Dept of Electronics and Communication Engg. BIT, Bangalore From 18th to 23rd February 2005
4	VLSI Design using Cadence Tools	Four day workshop	Sri Venkateshwara College of Engg	SVCE, Bangalore 27th February to 2nd March 2006
5	Cadence-VTU VLSI Lab Training	Tools training	Cadence Design systems	3rd March 2006
6	Cadence-Tools Training	Tools training	Cadence training center	20th september 2007
7	Recent trends in VLSI and Embedded System Design Technology	Two day workshop	Global Academy of Technology in association with CADENCE and UTL technologies	Dept of Electronics and Communication Engg.GAT, Bangalore From 12th to 13th April 2007
8	Analog and Mixed mode Design using Cadence Tool	Three day workshop	BNMIT and CADENCE, Design systems	Dept of Electronics and Communication Engg.BNMIT Bangalore 2nd to 4th February 2009
9	VLSI, MEMS, and Integration	One day National Level workshop	VIT, Chennai	School of electronics Engineering, VIT, Chennai. 09-10-2011

10	FPGA Based Embedded System Design	One day Seminar	JSSATE in collabration with Dexcel EmDAC	Dept of Electronics and Communication Engg. JSSATE, Bangalore On 3rd January, 2012
11	International conference on VLSI Design 11th International conference on Embedded Systems	five day	Hyderabad International Convention Center, Hyderabad	7th to 11th January, 2012
12	National conference on Antennas and its applications	Two day	VTU, Belguam	VTU, Regional center, Bangalore 24th to 25th February, 2012
13	Advanced trends in Low Power SoC VLSI Design	Two day Workshop	Jain University	Center for Emerging Technologies, NGIT, Bangalore 5th - 6th October 2012
14	Advanced VLSI Design using Cadence Tool Suite	Three day FDP	Cadence Design Systems India Pvt. Ltd	Dept of Electronics and Communication Engg. JSSATE, Bangalore 16th to 18th July, 2014
15	National conference on VLSI, Signal and Image processing,	Two day National conference on NCVSIP-2014	JSSATE	Dept of Electronics and Communication Engg. JSSATE, Bangalore 22nd & 23rd August 2014
17	Signal , Image processing and SDR using Lab View	Two day Workshop	JSSATE in association with TECHLABS	Dept of Electronics and Communication Engg. JSSATE, Bangalore 22nd to 24th June, 2015
18	International conference on Signal and Image processing,	Three day conference on ICSIP-2014	BNMIT	BNMIT 8th to 10th January, 2014
19	2nd International conference on Nanomaterials and Technologies (CNT-2014)	Two day conference	Vardhaman college of engineering, Hyderabad	Research and development centre,Department of electronics and communication Engineering Vardhaman college of engineering, Hyderabad, 17-18 october 2014
20	workshop on Design verification using verilog and system verilog	Two day workshop	JSSATE in association with EDULIFE	Department of electronics and communication Engineering, JSSATE Bangalore, 26-27 Nov 2015