



JSS MAHAVIDYAPEETHA

JSS ACADEMY OF TECHNICAL EDUCATION

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1. **NAME** : kavitha M
2. **Designation** : Assistant Professor
3. **Name of the Dept.** : Electronics & Communication Engineering
4. **Date of joining the Institution:** 27-12-2001
5. **Date of Birth** : 10-08-1977
6. **Father's Name** : MahadevaSwamy
7. **Sex** : Female
8. **Nationality** : INDIAN
9. **Contact No.** : 9449238353
10. **E-mail ID** : **mkavithajss@gmail.com**
 - a. **Correspondance** : Asst.Professor, Department Of ECE,
JSS ACADEMY OF TECHNICAL EDUCATION,
UTTARAHALLI – KENGERI MAIN ROAD,
BENGALURU 560060
 - b. **Permanent Address** : #3035,14th cross, 6th main,
BSK-II Stage, Bangalore-560070
11. **Employment Type** : Permanent
12. **Educational Qualifications** : **B.E., M.Tech., (Ph.D.)**,
(In reverse Chronological Order)



Sl. No	Degree	Branch	Specialization	Year of passing	University
1	(Ph.D)	Electronics & Communication Engineering	VLSI Design	Persuing	VTU, Belgaum
2	M.Tech	Electronics & Communication Engineering	VLSI Design and Embedded Systems	2007	VTU, Belgaum
3	B.E	Electronics & Communication Engineering	Electronics & Communication Engineering	1999	Bangalore

13. Service / Experience Details : 16 years
(In reverse Chronological Order)

a. Teaching Experience:

Sl. No.	From (dd-mm-yy)	To (dd-mm-yy)	No. of years	Degree or Diploma Institution	Designation	Name of the Institute
1	12-05-2008	Till date	8.2Years	Degree	Assistant Professor	JSS Academy of Technical Education, Bengaluru 560 060
2	01-01-2007	11-05-2008	1.5 Years	Degree	Senior Lecturer	JSS Academy of Technical Education, Bengaluru 560 060
3	27-12-2001	31-12-2006	6 Years	Degree	Lecturer	JSS Academy of Technical Education, Bengaluru 560 060
4	15-11-2000	07-02-2001	3 months	Degree	Lecturer	PES College of Engineering, Mandya
Total Experience				16 Years		

b. Industrial Experience:

Sl. NO	From	To	No. of years	Designation	Name of the Company
1					

14. Membership in various University Boards / Committees / Other (Specify):

Sl. No.	Body	From	To	Name of the University / Institution / Organisation
1	Board of Examiners	NA		
2	Board of Studies	NA		
3	Academic Senate	NA		
4	Executive Council	NA		
5	LIC	MPCC	NA	

15. Awards : Nil

16. Details of Books published : Nil

17. Number of Ph.D. Guidance : Nil

18. Field of Expertise / Interest : VLSI Design, Communication,
Digital Circuits & Logic Design

19. Patents : Nil

20. Projects

Sl. No.	Name of the project	Principal Investigator / Co-Investigato	Amount sanctioned From	Amount	Date of start of the project	Date of completion of the project	Outcome of the project
1							
2							
3							
4							

21. Details of Publications:

Google scholar link: <https://scholar.google.co.in/citations?hl=en&imq=kavitha+m&user=jc7XKy8AAAAJ>

As on 30-08-2016

Citation Indices	All	Since 2011
Citations	NIL	NIL
h-Index	NIL	NIL
i10-Index	NIL	NIL

Number of papers published in International Journals : 03

Number of papers published in National Journals : Nil

Number of papers published in International Conferences : 02

Number of papers published in National Conferences : 03

a. Journals: International

Sl. No.	Name of Co-Author	Title of Paper	Name of the Journal	Publisher	Publication citation ISSN, ISBN, Vol. No., Issue, pp
1	Kavitha M	FPGA Implementation of Four-Channel Bit Error Rate Tester for Spacecraft Data Acquisition System	International Journal of Information Technology and Computer		e- ISSN : 2455-529 Month & Year : 2016 Page Nos. : 109-113

			Engineering		
2	Kavitha M	Design and Performance analysis of a Low Power First order sigma Delta modulator	International Journal of Applied Engineering Research		Online ISSN : 0973-4562 Volume No. : 10 Issue No. : 92 Month & Year : 2015 Page Nos. : 284-290
3	Kavitha M	An 8-bit area optimized low power continuous time band pass sigma-delta ADC in 45nm CMOS	International Journal of Engineering Research		Online ISSN : 2319-6890 Volume No. : 4 Issue No. : 3 Month & Year : May 2015 Page Nos. : 155-159

b. Journals: National

Sl. No	Name of Co-Author	Title of Paper	Name of the Journal	Publisher	Publication citation ISSN, ISBN, Vol. No., Issue, Impact Factor, pp
1					
2					

c. Conferences: International

Sl. No	Name of Co-Author	Title of Paper	Name of the Conference	Publisher	Publication citation ISSN, ISBN, Vol. No., Issue, pp
1	Kavitha M	Design and Performance analysis of a Low Power First order sigma Delta	International Conference on Researches in		

		modulator	Science, Management and Engineering		
2	Kavitha M	An 8-bit area optimized low power continuous time band pass sigma-delta ADC in 45nm CMOS	2 nd International Conference on Convergent innovative Technologies ICCIT-2015 held at Cambridge Institute of Technology, Bangalore		Online ISSN : 2319-6890 Volume No. : 4 Issue No. : 3 Month & Year : May 2015 Page Nos. : 155-159

d. National conferences / Symposium / workshops

Sl. No	Name of Co-Author	Title of Paper	Name of the Conference	Publisher	Publication citation ISSN, ISBN, Vol. No., Issue, pp
1	Kavitha M	FPGA implementation 4-channel bit error rate tester for space trak data aquasition system	NCRASET-16		SVCE,B'LORE
2	Kavitha M	“Design and Verification of Difference-Set codes for memory application”.	Second National Conference on “Wireless Control& Communication Technologies(NCWC T-2014).	24 th -25 th April 2014	Organized by Department of TCE at Dr.AIT, Bangalore.
3	Kavitha. M	Interlaken protocol to SPI – 4.2 bridge with emphasis on low power	NEWS- 2012, BMSCE, Bangalore	3 rd and 4 th August 2012	Organized by Department of Electronics & Communication Engineering, BMSCE, Bangalore